# Introduction

The FIFO\_CDC is a First In First Out core with Clock Domain Crossing capabilities. The core is configurable to holding data in 8, 16, 24, and 32 bit vector sizes with associated FIFO depths of 2048, 1024, 512, and 512. The data width can be changed at runtime with an associated wipe of the FIFO contents and a period of no operation. The domain that acts as the control signal master is selectable with a VHDL generic.

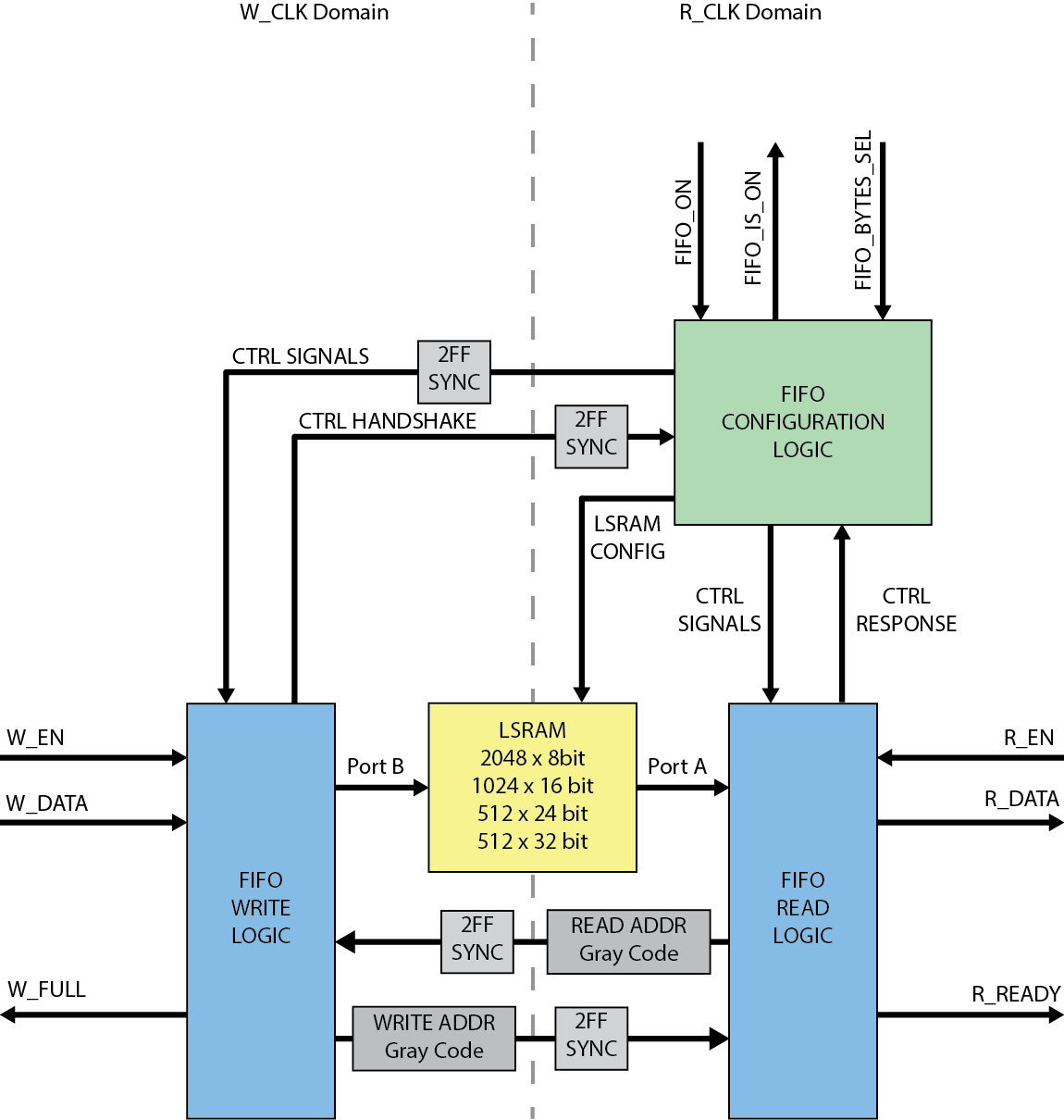


Figure 1 FIFO block diagram with R\_CLK control

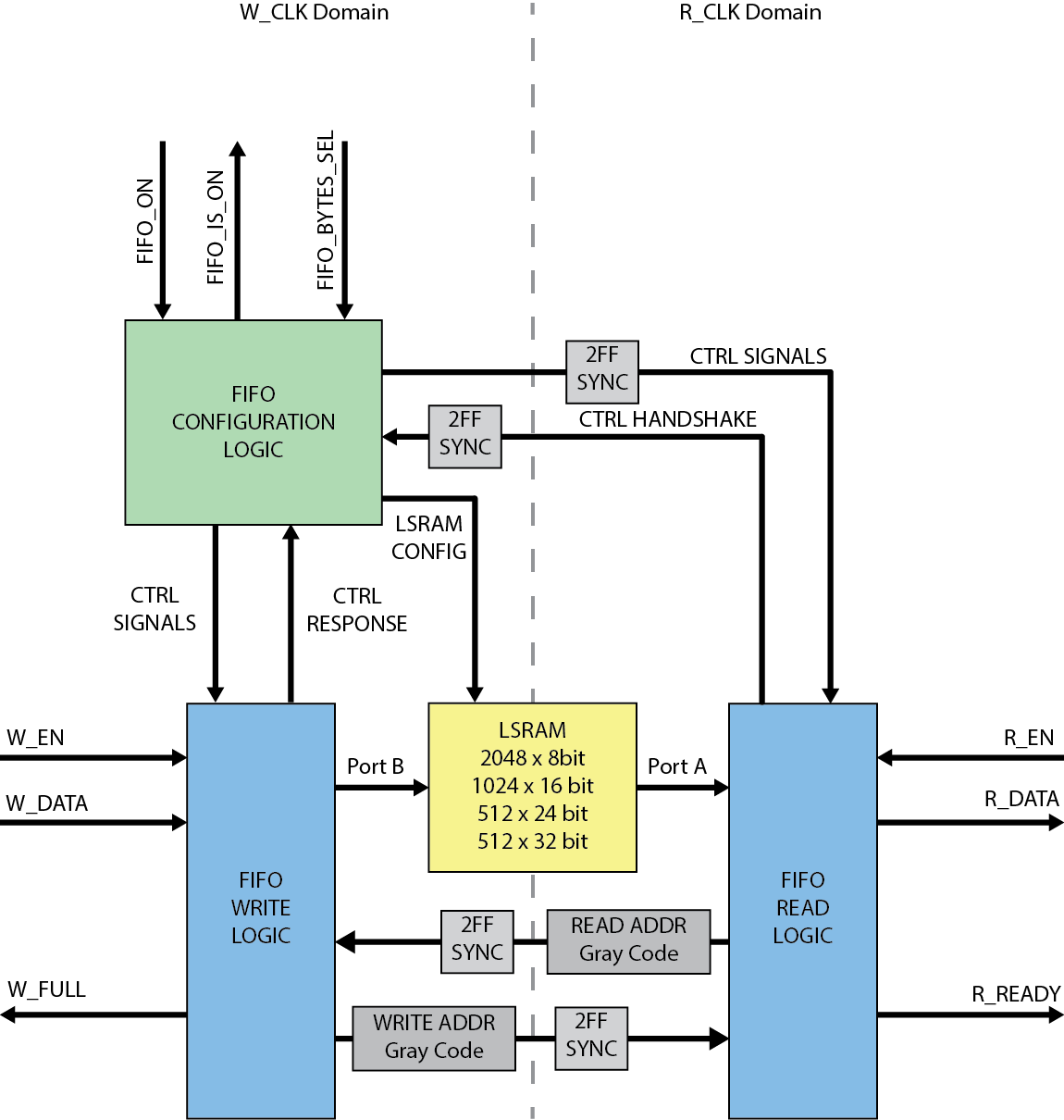


Figure FIFO block diagram with W\_CLK control